UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,188	04/04/2005	Tatsuya Iwasaki	03500.018068	9606

5514 7590 07/28/2006

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
KIANNI, KAVEH C	

ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/530,188	IWASAKI, TATSUYA	
	Examiner	Art Unit	
	Kianni C. Kaveh	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *8 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *8 and 9* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

Group 1, claim(s) 1-7, drawn to a reconfigurable optoelectronic circuit including a plurality of logic blocks of electronic circuit and an optical circuit interconnecting them, wherein both the internal configuration of each of the logic blocks and the optical interconnections of the logic blocks using the optical circuit are alterable (see related figures such as FIG. 4).

Group 2, claim(s) 8 drawn to a hierarchically reconfigurable circuit including second stratum containing logic blocks having electric wires and switches arranged in the form of a matrix (shown in fig. 3).

Group 3, claim 9, drawn to an interconnection structure including ports connected to the logic elements and adapted to perform opto-electric signal conversions and a means for altering optical interconnections among the ports by way of a sheet-shaped optical transmission medium (fig. 12-14).

The inventions listed as Groups 1, 2 and 3 do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: each of the above group inventions directed to an invention that is distinct, and requires a different search, than that of other inventions; in which group 2 is combination that include sub-

optoelectronic structures in which groups 1 and 2 can be considered subcombination each having distinct sub-optoelectronic structure that can be used in the combination structure of invention I.

During a telephone conversation with (John Mayluan for Jason Okum) on 6/6/06 a provisional election was made without traverse to prosecute the invention of 1, claims 1-7. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8-9 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 2, 4 and 5 recites the limitations: 'the internal configuration' and 'optical interconnections' in claim 1, 'the inter-port' in claim 2, the logic elements in claim 4, the configuration data in claim 5. There is insufficient antecedent basis for these limitation in the claim. Corrections are required.

Claims 1 are ambiguous, since "signal to or receive' in claim 2, 'blocks can be' in claim 3, 'elements is or' in claim 4, 'copy and/or' in claim 7 are not undefined. The applicant need to specify which limitations within the claimed invention pertain the above

elements and whether an element does some specific function rather than stating such limitations as 'block can' or 'copy and/or'. Appropriate corrections are required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saleh et al. (US 6982974).

Regarding claim 1, Saleh teaches a reconfigurable optical and electronic circuitry (shown in fig. 13; see abstract) adapted to alter its internal configuration (the limitations adapted and its relevant sequenced limitations are not given patentable weight since

it has been held that the recitation that an element is "adapted to" perform a function is not a positive

limitation but only requires the ability to so perform. it does not constitute a limitation in any patentable sense. In re Hutchison, 69
USPQ I38.; however, this limitation is taught by Saleh see at least abstract);

comprising

a plurality of logic blocks of electronic circuit and an optical circuit interconnecting them (see col. 10, 3rd parag., wherein optical circuits interconnecting them, see at least abstract and col. 7, 3rd parag.),

wherein both the internal configuration of each of the logic blocks and the optical interconnections of the logic blocks using the optical circuit are alterable (see abstract and col. 10 1st and 3rd parag.; also at least col. 5, 1st parag, and fig. 21 and its description; wherein interconnections can be made/added/removed/altered through optical means such as optical fiber and the connections can be electrical and/or optical see col. 7, 3rd parag.).

However, Saleh does not explicitly state optoelectronic circuit. It is obvious/well-known to those of ordinary skill in the art when the invention was made that optical and electrical circuitry used in a communication network is/known-as optoelectronic circuit, since such configuration would provide matrix synchronization with low loss and cost (col. 4, 2nd parag.)

Regarding claims 2-7, Saleh further teaches wherein said optical circuit includes a sheet-shaped optical transmission medium and ports (see col. 10, 1st parag. and also shown in at least fig. 1, items optical transceivers, also optical SONET configurations in fig. 1b) adapted to at least either transmit an optical signal to or receive an optical signal from the optical transmission medium, the inter-port optical connections being

arranged so as to allow alterations (the limitations adapted and its relevant sequenced limitations are not given patentable weight since it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. it does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ I38.; however, this limitation is taught by Saleh see at least fig. 1 and relevant descriptions); wherein closely located ones of the logic blocks can be interconnected by electric wires (see at least col. 10, 1st parag.); wherein each of said logic blocks includes a plurality of logic elements and an electric connection network interconnecting the logic elements and at least either the internal configuration of at least one of the logic elements is or the interconnections of the logic elements are alterable (see abstract and col. 10 1st and 3rd parag.; also at least col. 5, 1st parag, and fig. 21 and its description; wherein interconnections can be added/removed/altered through optical means such as optical fiber and the connections can be electrical and/or optical see col. 7, 3rd parag.); wherein configuration data are distributed by way of said optical circuit and the internal configuration of any of the logic blocks is altered according to the configuration data (see abstract and col. 10 1st and 3rd parag.; also at least col. 5, 1st parag, wherein configuration data are also through reprogramming/writing and/or moving data); wherein each of said logic blocks comprises a variable logic section and a memory section and the memory section holds configuration data that corresponds to the internal configuration of the variable logic section (see col. 34, 2nd parag.); wherein said logic blocks are adapted to move, copy and/or replace the internal configuration of some other logic block

by way of the optical circuit (the limitations adapted and its relevant sequenced limitations are not given patentable weight since it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. it does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ I38.; however, this limitation is taught by Saleh see at least col. 34, 2nd prarag.).

Citation of Relevant Prior Art

Prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In accordance with MPEP 707.05 the following references are pertinent in rejection of this application since they provide substantially the same information disclosure as this patent does. These references are:

US 6289440 B1 Casselman; Steven
US 6016211 A Szymanski; Ted et al.

These references are cited herein to show the relevance of the apparatus/methods taught within these references as prior art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to K. Cyrus Kianni whose telephone number is (571) 272-2417.
The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 6:00 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font, can be reached at (571) 272-2415.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or:

Hand delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956.

KAVEH KIANNI
PRIMARY EXAMINER

K. Cyrus Kianni
Primary Patent Examiner
Group Art Unit 2883

July 20, 2006